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09/595,198	06/16/2000	Marc Fleischmann	TRANS39	1109

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EXAMINER
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ART UNIT	PAPER NUMBER
2185	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/595,198	FLEISCHMANN ET AL.	
	Examiner	Art Unit	
	Mark Connolly	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 September 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Objections

1. Claim 6 is objected to because of the following informalities: Applicant refers to a *said processor* while talking about a *host processor* and a separate *virtual target processor*. It is unclear which processor the *said processor* refers to. Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 6 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

3. Claim 6 recites the limitation "said processor" while explaining both a host processor and a virtual target processor. It is unclear which processor the "said processor" refers to. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-2, 4-5, 7-9 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakai U.S. Pat. No. 6266776 in view of Applicants Admitted Prior Art [AAPA].

5. Referring to claim 1, Sakai teaches the invention substantially including:

a. determining if a prescribed period of inactivity has been attained [col. 6 lines 56-58]. The prescribed period of inactivity is interpreted to be the period of time to enter the S2 sleep state.

b. removing all electrical power from the processor, whereby the processor is powered down, notwithstanding continued supply of electrical power to the computer [col.1 lines 39-42].

c. restoring electrical power to the processor when processing is to resume [col. 1 lines 59-64]. It is inherent that when processing is to resume, there would be a return to the S0 state (the ON state).

Sakai does not explicitly teach preserving the internal context against loss due to removal of electrical power from the processor in response to an affirmative determination of the period of inactivity, nor does Sakai explicitly teach restoring the preserved internal context to the processor then the processing is to resume. Even though Sakai does teach preserving system contents when entering a sleep state and restoring the system contents when returning to the ON state, the system context is not explicitly taught to comprise CPU context. In summary, Sakai does not explicitly teach preserving and restoring the context to the processor when entering and returning from a sleep mode.

AAPA does explicitly teach preserving and restoring the context to the processor when entering and returning from a sleep mode [page 4 lines 1-7]. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Sakai to preserve and restore the CPU context to the processor when entering and returning from a sleep mode because the AAPA teaches that it is desirable to preserve the processor context when entering an STR sleep mode

(i.e. a sleep mode where the power is removed from the processor. page 3 lines 14-15) so that the context is available for later use when restoring the processor from the sleep mode.

6. Referring to claim 2, AAPA teaches reading the internal context from the internal memory of the processor prior to removal of electrical power from the processor and writing the context into a second memory which is electrically powered separately from the processor [page 3 lines 12-19]. It is inherent that the context is read prior to the removal of power to the processor, otherwise the data would be lost and unrecoverable before it could be written into the second memory.

7. Referring to claims 4 and 5, AAPA teaches initializing the processor and determining if the power was removed due to a power on reset or an STR. AAPA also teaches that if it has been determined that the power removal was due to an STR to access and install the preserved processor context [page 4 lines 13-21].

8. Referring to claim 7, Sakai teaches the invention substantially including:

a. a CPU for processing instructions of an application, the CPU including internal registers. It is well known that CPU's include internal registers.

b. a first and second memory [col. 1 lines 49-51]. The non-volatile storage is interpreted to be the first memory and the system memory is interpreted to be the second memory. In addition, memory is interpreted as something that stores information.

c. a power supply for supplying power separately to the CPU and the first and second memory [col. 1 lines 39-41 and lines 49-51]. It can be seen that in the S2 state that the CPU is powered down separately from the first and second memories. It isn't until later in the S4 state that the first and second memories are powered off.

d. a power supply including a battery [col. 1 lines 13-14].

e. a first and second power circuit means for distributing electrical power to the CPU and the first and second memories respectively. It is inherent that Sakai comprises a first and second power means to distribute power to the CPU and first and second memories respectively.

f. an on-off switch for closing power from said battery to each of the first and second power circuit means whereby the first and second power circuit means is enables to deliver power. This on-off switch is interpreted as a main power on/off switch, which is located on the outside of virtually every computer system. It is inherent that Sakai comprises an on-off switch.

g. a first program routine means for detecting inactivity of application instruction processing of the CPU for a period of time [col. 6 lines 56-58].

Sakai does not explicitly teach:

a. a second program routine means for saving the entire internal context of the CPU in the second memory and for producing an STR signature in response to a positive detection of inactivity by the first program routine means

b. a third program means for terminating distribution of power by the first power circuit means following completion of the second program routine means, whereby power is removed from the CPU while the internal context of the CPU is preserved in the second memory.

AAPA teaches:

a. a second program routine means for saving the entire internal context of the CPU in the second memory and for producing an STR signature in response to a positive detection of inactivity by the first program routine means [col. 4 lines 1-4 and 13-16]. The DRAM memory and system memory of Sakai are interpreted to be the same. In addition, it is obvious that the AAPA would produce an STR signature because it provides a way for the operating system to determine if an STR occurred so that it can Resume from STR.

b. a third program means for terminating distribution of power by the first power circuit means following completion of the second program routine means, whereby power is removed from the CPU while the internal context of the CPU is preserved in the second memory [page 3 lines 23-25 and page 4 lines 1-4].

It would have been obvious to one of ordinary skill in the art to modify Sakai to include the teachings of AAPA because the AAPA teaches that it is desirable to preserve the processor context when entering an STR sleep mode (i.e. a sleep mode where the power is removed from the processor. page 3 lines 14-15) so that the context is available for later use when restoring the processor from the sleep mode.

9. Referring to claim 8, the AAPA teaches:

a. a user operated input device for enabling user input to the application and means for enabling the second power circuit means to distribute power to the CPU, responsive to operation of the user operated input device [page 2 lines 22-25]

b. program means responsive to re-energization of the CPU for initiating an initialization process for the CPU [page 4 lines 8-12].

c. loading and processing a boot loader [page 4 lines 9-10]. It is well known that the normal boot-up routine stored in a ROM of the BIOS comprises loading and processing a boot loader.

d. configuring internal memory of the CPU, excluding the second memory and resetting the registers of the CPU [page 4 lines 11-12]. It is obvious that the second memory would not be configured along with the memory of the CPU because if it was, then the CPU context which is stored in the second memory would become corrupt or even lost.

e. checking for an STR signature [page 4 lines 13-16]. It is obvious that the system would check for the STR signature in order to determine if the loading of the operating system was due to an STR.

f. retrieving the portion of the internal context of the CPU earlier stored in the internal memory of the CPU and reading back the portion into the registers of the CPU [page 4 lines 16-19].

AAPA does not explicitly teach that the context of the Northbridge [NB] registers are retrieved and loaded into the CPU but it is obvious that this does occur because the AAPA further teaches that "the CPU can proceed with executing the next application program instruction exactly where the CPU left off when entering STR" [page 4 lines 21-23]. Because the CPU communicates via the NB, it is obvious that the context of the NB would be loaded into the CPU.

10. Referring to claim 9, the AAPA teaches retrieving the next instruction of the application program [page 4 lines 21-23].

11. Referring to claim 12, AAPA teaches the invention substantially including:

a. a CPU

b. private memory [page 4 lines 1-4]. The private memory is interpreted to be the same as well defined location in the DRAM.

c. a power supply

d. the power supply for supplying power to the CPU and the private memory independent of one another to enable withdrawal of power from the CPU without withdrawal of power from the private memory [page 4 lines 5-7].

e. the CPU defining and maintaining a CPU context to enable processing of application programs and the CPU context being stored in the private memory whereby the context is retained upon withdrawal of power from the CPU without withdrawal of power from the private memory [page 4 lines 1-7].

12. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sakai and AAPA as applied to claims 1-2, 4-5, 7-9 and 12 above, and further in view of Sasscer U.S. Pat. No. 4523206.

13. Referring to claim 3, it is obvious and well known in the art that a processors internal memory includes a cache memory. The Sakai-AAPA system does not explicitly teach powering the cache separately from the processor so that when the power to the CPU is removed, power to the cache will be maintained. Sasscer teaches that it is desirable to supply power to the cache so when power is removed from the processor, the power to the cache is unaffected and prevents the loss of the context of the cache (i.e. memory contents) [col. 5 lines 54-60]. It would be obvious to one of ordinary skill in the art at the time of the invention to modify the cache in the

CPU to include a powering means, separate of that from the CPU, to prevent the loss of context of the cache upon removal of power to the processor because it would provide a means to prevent losing the CPU context when power is suddenly removed from the CPU.

14. Claim10 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakai and AAPA as applied to claims 1-2, 4-5, 7-9 and 12 above, and further in view of Tanenbaum.

15. Referring to claim 10, this is rejected on the same basis as set forth in the rejection for claim 7 with the exception that the Sakai –AAPA system does not explicitly teach a code morphing program means defining a virtual X86 processing system. The Sakai –AAPA system does not explicitly teach a virtual X86 processing system including a virtual X86 CPU and virtual Northbridge chip where the instructions of the X86 application program may be processed in the processing system. In summary, the Sakai – AAPA system does not explicitly teach software versions of the CPU and Northbridge chip to execute the instructions of the X86 application program.

Tanenbaum teaches "Hardware and software are logically equivalent" [page 11 line 11]. Tanenbaum then goes further and teaches that hardware can be simulated in software [page 11 line 13]. Therefore it would have been obvious to one of ordinary skill in the art to modify the Sakai –AAPA system to include a virtual CPU and Northbridge because both can perform the same operations. Furthermore, an artisan would also be motivated to create a virtual CPU and a virtual Northbridge because it would reduce the size and cost of a system in comparison to a system where the same CPU and Northbridge was realized in hardware.

16. Referring to claim 11, this is rejected on the same basis as set forth hereinabove.

17. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sakai and AAPA as applied to claims 1-2, 4-5, 7-9 and 12 above, and further in view of Song et al U.S. Pat. No. 5991531.

18. Referring to claim 13, the Sakai – AAPA system as described above does not explicitly teach the computer comprising a host computer for dynamically translating and executing instructions of a target application designed for processing by a target computer containing an instruction set different from the instruction set of the host computer. In summary, the Sakai – AAPA system does not teach translating and executing instructions, which are designed to run on a separate computer, to run on a host computer. Song et al does explicitly teach translating and executing instructions, which are designed to run on a separate computer, to run on a host computer [col. 1 lines 45-52, col. 3 lines 26-29 and 35-39]. The vector processor architecture that permits emulation of double-width operations is interpreted as the host computer. The 64-byte operations are interpreted as the instruction set designed for processing by a separate target computer and which is also different from the instruction set of the host computer. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the Sakai – AAPA system to allow the emulation and process of instructions that are designed to run on a separate computer because it would allow the Sakai – AAPA system to support the longer data width operations, which are more common in newer processors, while still maintaining a reduced chip size, cost and code length as taught by Song et al [col. 2 lines 41-43].

19. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sakai in view of Gilgen U.S. Pat. No. 6182231.

20. Referring to claim 14, Sakai teaches a method of initiating different sleep states that are activated under different conditions. Sakai further explains that a PC would be placed into an S1 (non-STR) stage when for example a user leaves the office. If additional power savings were needed, then the S1 stage would transition into an S3 (STR) stage [col. 2 lines 29-41]. Sakai does not teach intercepting an issued sleep instruction and determining if the issued instruction should be substituted with a different sleep instruction.

Gilgen teaches a power management program that intercepts an issued sleep instruction, makes a determination about the sleep instruction and modifies the issued sleep instruction to improve efficiency [col. 1 lines 35-38, 53-55, col. 4 lines 55-59 and Fig. 2]. It would have been obvious to one of ordinary skill in the art at the time of the invention to realize that substituting the sleep instruction and modifying the sleep instruction perform the same basic task which is to initiate a sleep instruction different from that being issued from a power management program.

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Sakai by intercepting the issuance of the S1 sleep state (pre-STR) and issue an S3 sleep state (STR) when a user left the office because it would improve efficiency of the PC by placing it in a more optimal power saving mode.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. U.S. Pat. No. 5204963 to Noya. This teaches a backup power supply to retain the contents of a cache.

b. U.S. Pat. No. 5671229 to Harari et al. This teaches having a separate power supply to the cache to maintain memory long enough to dump contents into another memory.

c. U.S. Pat. No. 6397242 to Devine et al. This teaches a virtual computer system with a virtual processor.

d. U.S. Pat. No. 6405320 to Lee et al. This teaches maintaining bit patterns which identify the current power saving mode.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mark Connolly whose telephone number is (703) 305-7849. The examiner can normally be reached on M-F 8AM-5PM (except every first Friday).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C Lee can be reached on (703) 305-9717. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Mark Connolly
Examiner
Art Unit 2185

THOMAS LEE
SUPERVISORY PATENT EXAMINER
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March 18, 2003
MC